

IN THE SPECIFICATION:

Please amend the specification as follows:

Paragraph 0035: please replace this paragraph with the following rewritten paragraph:

In a particular embodiment, first etch layer 34 30, which may be a dielectric or a conductor, as shown in FIG. 12, may be formed over emission layer 20 and tips 24. First etch layer 34 30 may comprise aluminum or a dielectric etchable material and can be formed through sputter deposition or other common techniques. First intermediate dielectric layer 120 may be formed over first etch layer 34 30 and may comprise silicon nitride, a stable silicon dioxide, or other dielectric material that is capable of being selectively etched in relation to first etch layer 34 30 or layers formed later in time. First intermediate dielectric layer 120 may have a thickness in the range from about 0.1 to about 0.7 micron, for example. Second intermediate dielectric layer 122 can be formed over first intermediate dielectric layer 120 and may comprise silicon dioxide or other dielectric material that is capable of being selectively etched in relation to first etch layer 34 30, first intermediate dielectric layer 120, or layers formed later in time. The second intermediate dielectric layer may have a thickness in the range from about 0.5 to about 1.5 micron, for example. Support layer 32 is formed over the second intermediate layer and may comprise silicon nitride, a stable silicon dioxide, or other dielectric material that may be selectively etched in relation to first etch layer 34 30, first intermediate dielectric layer 120, second intermediate dielectric layer 122, or layers formed later in time. First intermediate dielectric layer 120, second intermediate dielectric layer 122, and support layer 32 can be formed through chemical vapor deposition or other conventional methods. Gate layer 34 may be formed over the support layer as described above. Preferably, all of these layers may each

have a total thickness in the range of about 0.5-3 micron, but other values of thickness can also be used.

Paragraph 0036: please replace this paragraph with the following rewritten paragraph:

Photoresist can be applied and gate layer 34 and support layer 32 may be etched as described above to form an opening in layer 32 and to expose second intermediate dielectric layer 122 through that opening. The opening in support layer 32 should be equal in size or smaller in size than the opening in gate 34. A wet etch, such as buffered hydrofluoric acid or another similarly reactive chemical, may then be used to etch second intermediate dielectric layer 122 between support layer 32 and the first intermediate dielectric layer 120 to form cavity 130 between support layer 32 and first intermediate layer 120, illustrated in FIG. 13. A reactive ion etch, as described above, can then etch first intermediate layer 120 to expose first etch layer 34 30. A wet etchant, such as phosphoric acid or another similarly reactive chemical, can be used to remove first etch layer 34 30 from tips 24 resulting in the structure illustrated in FIG. 14. First etch layer 34 30 may be etched completely away from most tips 24 to form a cavity (not shown).